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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/810,037
Filing Date: March 26, 2004
Appellant(s): PURDY, MATTHEW A.

Scott F. Diring, Reg. No. 35,119
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 8/24/07 appealing from the Office action mailed 5/21/07.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,751,519	SATYA ET AL	06-2004
2003/0060916	HSIEH	03-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-5, 7-8, 10-18, 20-21 and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satya et al. (6,751,519) in view of Hsieh (2003/0060916).

Regarding claim 1:

Satya teaches receiving fault classification data associated with a fault condition (col. 4 lines 47-53 and lines 64-67); and

estimating at least one yield parameter of the wafer based on the fault classification data (col. 4 lines 64-67).

Satya does not explicitly teach the fault data being associated with a tool fault condition that is associated with a process tool for processing a wafer. Satya does, however, teach examining defects and classifying the defects of a wafer.

Hsieh teaches that defect data of a wafer is associated with a process tool fault condition that is associated with a process tool for processing a wafer (paragraphs 0026 and 0028 – if a wafer contains defects, it is determined which machine processed the wafer).

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the process tool association of Hsieh with the defect data and yield prediction of Satya.

One of ordinary skill in the art at the time of invention would have been motivated to make the combination because Hsieh teaches that associating the process tool fault

condition with the defect data allows for the process tool to be calibrated to lower the possibility of defect occurrence (paragraph 0028).

Regarding claim 2:

Satya teaches:

wherein estimating the at least one yield parameter further comprises estimating an overall yield parameter (col. 5 lines 14-16 and col. 7 line 65-col. 8 line 2).

Regarding claim 3:

Satya teaches:

wherein estimating the overall yield parameter further comprises estimating a number of die lost (col. 7 line 65-col. 8 line 2 – estimating final wafer yield inherently includes estimating a number of die lost).

Regarding claim 4:

Satya teaches:

wherein estimating the overall yield parameter further comprises estimating a percentage of die lost (col. 7 line 65-col. 8 line 2 – the number of dice are known. If a final yield is estimated, simply dividing the estimated final yield by the total gives the percentage).

Regarding claim 5:

Satya teaches:

wherein estimating the at least one yield parameter further comprises estimating a performance yield parameter (col. 11 lines 12-47 – estimating failure probability clearly reads on a performance parameter prediction).

Regarding claim 7:

Satya teaches:

wherein estimating the at least one yield parameter further comprises associating at least one estimated yield parameter with a fault class specified by the fault classification data (col. 4 lines 64-67 and col. 12 lines 17-36).

Regarding claim 8:

Satya teaches:

determining an actual yield parameter for a wafer (col. 8 lines 61-66); and

updating the estimated yield parameter based on the actual yield parameter (col. 8 lines 61-66).

Regarding claim 10:

Satya teaches:

further comprising scrapping the wafer responsive to the estimated yield parameter being outside a predetermined range (col. 8 lines 38-44).

Regarding claim 11:

Satya teaches:

determining process/step data associated with the tool fault condition (col. 7 line 65-col. 8 line 2); and

estimating at least one yield parameter based on the fault classification data and the process/step data (col. 7 line 65-col. 8 line 2).

Regarding claim 12:

Satya teaches:

further comprising estimating a plurality of yield parameters based on the fault classification data and the process/step data (col. 7 line 65-col. 8 line 2).

Regarding claim 13:

Satya teaches:

further comprising estimating a plurality of yield parameters based on the fault classification data (col. 7 line 65-col. 8 line 2).

Regarding claims 14-18, 20-21 and 23-27:

The claims are rejected as the systems for performing the methods of claims 1-5, 7-8 and 10-13.

Claims 9 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satya and Hsieh as applied to claims 1 and 14 above and further in view of Atkinson et al. (2004/0029029).

Regarding claims 9 and 22:

The teachings of Satya and Hsieh are outlined above.

Satya and Hsieh do not explicitly teach removing a process tool associated with a tool fault condition from service if the estimated yield parameter is outside a predetermined range. Satya and Hsieh do, however, teach taking necessary measures if an estimated yield parameter is outside a predetermined range.

Atkinson teaches removing a process tool associated with a fault condition from service if the estimated yield parameter is outside a predetermined range (paragraph 0026).

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the tool shutdown procedure of Atkinson with the manufacturing process of Satya and Hsieh.

One of ordinary skill in the art would have been motivated to make the combination because Atkinson teaches that shutting down a process tool avoids problems that threaten multiple lots of wafers (paragraph 0026).

(10) Response to Argument

Applicant argues, on pages 7 and 8:

"The combined references do not teach receiving fault classification data associated with a tool fault condition, where the tool fault condition is associated with a process tool for processing a wafer."

The examiner respectfully disagrees. Satya clearly teaches receiving fault data, this fault data including the defect type of the defect that has been determined on the wafer. The fact that a defect type is specified clearly teaches fault classification data, i.e. the defect is *classified* as a particular type of defect. The Hsieh reference teaches determining defect data of a wafer and then determining which tool was processing the wafer that contains the defect such that the tool processing the wafer can be isolated as the faulty tool in order to calibrate or shut down the tool to eliminate the faulty condition of the tool. Combined, the references clearly teach detecting a defect, determining the type of defect and associating that defect with a particular tool that produced the fault and needs correction. It is also clear to one of ordinary skill in the art that determining which tool is the faulty tool that is causing the particular defect type is equivalent too, and in fact is the very definition of, associating the fault classification data with a tool fault condition.

It would appear, from applicant's arguments, that applicant is asserting that having fault classification data associated with a tool fault condition requires that the fault classification data be a classification of the tool fault. In fact, applicant further argues steps that applicant seems to believe are required for the classification data to be produced, but which are not to be found anywhere in the claims. A careful reading of claims, however, will show that applicant has merely claimed fault classification data and has then claimed that the fault classification data is associated with a tool fault. Two items being associated with one another, by definition, means that they have some relation to one another. In this case, the determined defect type (fault classification data) is related back to the tool that created the defect (association) such that the tool can receive the necessary calibration (i.e., a tool fault condition is present). All elements of the claimed subject matter are clearly present in the combination of references.

Applicant argues, on page 8:

"Neither Satya nor Hsieh teach or suggest generating fault classification data for an identified fault condition, and then using that fault classification data to estimate yield parameters."

The examiner respectfully disagrees. Satya clearly teaches that yield is predicted based on a particular type of defect (see Satya, col. 4 lines 66-67).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Marc Duncan/

Primary Examiner, AU2113

Conferees:

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER